Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **Select**
2. **A0**
3. **B0**
4. **Y0**
5. **A1**
6. **B1**
7. **Y1**
8. **GND**
9. **Y2**
10. **B2**
11. **A2**
12. **Y3**
13. **B3**
14. **A3**
15. **Output Enable**
16. **VCC**

**.060”**

**.075”**

**2 1 16 15**

**14**

**13**

**12**

**11**

**7 8 9 10**

**3**

**4**

**5**

**6**

**GP5**

**MCHC157**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential: VCC**

**Mask Ref: MCHC157**

**APPROVED BY: DK DIE SIZE .060” X .075” DATE: 7/11/22**

**MFG: MOTOROLA THICKNESS .016” P/N: 54HC157**

**DG 10.1.2**

#### Rev B, 7/1